REMARKS

Applicants have amended claims 1, 3, 5, 10 and 13 and cancelled claim 6 from further consideration in this application. Applicants are not conceding in this application that those claims are not patentable over the art cited by the Examiner, as the present claim amendments and cancellations are only for facilitating expeditious prosecution of the allowable subject matter noted by the examiner. Applicants respectfully reserve the right to pursue these and other claims in one or more continuations and/or divisional patent applications.

On May 21, 2007 an Interview was held between Examiner John Tabone Jr. and Applicants representative Anthony Palagonia. Proposed amendments to claims 1, 3, 5, 10 and 13 were discussed. Incorporation of details from Applicants FIG. 2 into claims 1 and 10 was discussed. The Examiner indicated that the proposed amendments to claims 3 and 5 would overcome the objection to claims 3 and 5. Claim 6 has be canceled.

The Examiner objected to Figure 6 stating: "Figure 6 is objected to because in Box 295 the word 'limited' should be changed to 'limit'." In response, Applicants have corrected FIG. 6 as suggested by the Examiner.

The Examiner objected to the specification stating: "The disclosure is objected to because of the following informalities: Page 6, l. 12, 'NPG circuit scan chains by a bus 175 should be "NPG circuit scan chains 170 by a bus 175'." In response, Applicants have amended the paragraph as suggested by the Examiner.

The Examiner objected to claims 1-20 because of the following alleged informalities: the phrase "macro circuit" is missing a hyphen and should be written, "macro-circuit" for consistency. In response, Applicants have amended claims 1 and 10 to change "macro circuit" to "macro-circuit" as suggested by the Examiner.

The Examiner objected to claim 13 because the phrase "a predetermined number" should allegedly be changed to "a predetermined limit" to correspond to the specification. In response, Applicants have amended claims 13 to change "number" to "limit" as suggested by the Examiner.

The Examiner objected to claims 3, 5 and 6 because in the phrase "adapted to" the claim scope is not limited by claim language that suggests or makes optional but does not require steps to be performed, or by claim language that does not limit a claim to a particular structure. In response, Applicants have amended claims 3 and 5 to remove the phrase "adapted to" and have canceled claim 6.

The Examiner rejected claims 1-3, 5, 6, 9-12, 14, 19 and 20 under 35 U.S.C. § 102(b) as allegedly being anticipated by Shubat et al. (US-6,363,020), hereinafter Shubat.

The Examiner rejected claims 15 and 16 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Shubat et al. (US-6,363,020), hereinafter Shubat.

The Examiner rejected claims 4, 7, 17 and 18 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Shubat et al. (US-6,363,020), hereinafter Shubat in view of Seitoh (US-6,829,181), hereinafter Seitoh.

The Examiner rejected claim 8 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Shubat et al. (US-6,363,020), hereinafter Shubat in view of DiRonza et al. (US-6,757,204), hereinafter DiRonza.

The Examiner rejected claim 13 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Shubat et al. (US-6,363,020), hereinafter Shubat in view of DeBrosse et al. (US-5,610,867), hereinafter DeBrosse.

Applicants respectfully traverse the § 102 and § 103 rejections with the following

arguments.

35 U.S.C. § 102(b)

The Examiner rejected claims 1-3, 5, 6, 9-12, 14, 19 and 20 under 35 U.S.C. § 102(b) as allegedly being anticipated by Shubat et al. (US-6,363,020), hereinafter Shubat.

As to claim 1, the Examiner stated: "Shubat teaches a multiplicity of macro-circuits (memory instances 204A - 204D, Fig. 3A), each macro circuit having the same function, a fuse bank (Fuses Box 206, Fig. 3A) containing a multiplicity of fuses, the state of said fuses storing test data indicating at least which macro-circuits failed a test, and means for preventing utilization of failing macro-circuits during operation of said integrated circuit (registers 208A through 208D, Fig. 3A). (Abstract, Col. 2, l. 46 to col. 3, l. 37, col. 7, l. 47 to col. 8, l. 20, claim 1)."

Applicants respectfully preface their arguments by pointing point out the following teachings in Shubat et al.:

(1) In col. 7, line 65 to col. 8, line 5, "Each of the memory instances includes a prime or main memory array and a redundant portion in any known manner or organization. Preferably, the redundant portions are not required to be of the same size for the memory instances. Further, each of the memory instances is provided with a volatile storage element (e.g., registers 208A through 208D) whose size corresponds to the size of the redundant portion disposed therein.

(2) In col. 8, lines 15-20: "In accordance with the teachings of the present invention, the memory instances 204A-204D are daisy-chained with the fuse box 206 via a signal path 257, in addition to being coupled to certain enable and clock signals. As will be described in greater detail herein below, signals effectuated on these signal paths are used, upon power-up followed by a reset of the device 202, for transferring or scanning out the contents of the fuse elements in the fuse box to the volatile registers 208A-208D disposed in the memory instances 204A-204D, respectively. The contents of the individual registers 208A-208D are then used for effectuating row redundancy (wordline replacement) or column redundancy (bitline replacement wherein a redundant block of bitlines are selected and a faulty block of primary memory bitlines are de-

selected) in a particular memory instance." Applicants note, that in FIG. 3A of Shubat et al. it is the volatile registers 208A-208D that are actually daisy chained.

(3) In col. 9, lines 29-55: The fuse box 206 contains a plurality of fuses 302 for storing fuse information or fuse data pertaining to defective wordlines and bitlines of the memory instances. Further, as mentioned above, the fuse box 206 is also provided with a plurality of redundancy scan flip-flops 304 wherein the number of flip-flops (for example, K) preferably equals or is greater than the total number of all flip-flops disposed in the memory instances. The fuses 302 in the fuse box are used to initialize the flip-flops 304 with the fuse data upon power-up or reset. Once the flip-flops 304 are initialized, the data therein is scanned out into the memory using the same flip-flops as scan registers. Preferably, the fuses and FFs in the fuse box are organized as a fuse box register with K register elements depicted in greater detail in FIGS. 6A and 6B. During power-up or after blowing the fuses, the contents thereof (i.e., fuse data or fuse information) are shifted into the volatile flip-flops of the memory instances (i.e., the shifting mode) and the fuse box is deactivated thereafter to eliminate or reduce quiescent current through the fuses. The transferred fuse data in the flip-flops is then used for effectuating row or column redundancy as set forth in greater detail herein below. The fuses may preferably be organized into a number of fields (e.g., an arbitrary N), each fuse field corresponding to one memory instance. It should be apparent that the size of an individual fuse field is dependent upon the amount of redundancy provided in the memory instance associated therewith. "

Therefore, Shubat et al. does not and cannot test the entire array of each instance 204A-204D through registers 208A-208D, but just the redundant array elements of the instances. Further, Shubat et al. must test all redundant elements of all instances in series. Finally, Schubert cannot prevent utilization of an entire instance, only failing redundant elements of the instances.

Applicants respectfully contend that Shubat et al. does not anticipate claim 1, as amended, because Shubat et al. does not teach each and every feature of claim 1.

In a first example, Shubat et al. does not teach "each macro-circuit of said multiplicity of identical macro-circuits being a logic circuit." Applicants point out, Shubat et al. is limited to memory circuits.

In a second example, Shubat et al. does not teach "said scan multiplexer and control circuit including means for selectively connecting said scan-in I/O pads and scan-out I/O pads to and disconnecting said scan-in I/O pads and scan-out I/O pads from each of said macro-circuits of said multiplicity of identical macro-circuits during testing of said multiplicity of identical macro-circuits." Since the registers 208A through 208D are fixed in a daisy chain there is no "means for selectively connecting" in Shubat et al. as required in Applicants claim 1.

In a third example, Shubat et al. does not teach: "means for isolating each macro-circuit of said multiplicity of macro-circuits from any other logic circuits of said integrated circuit chip and means for connecting scan-in and scan-out pins dedicated to each macro-circuit of said multiplicity of macro-circuits to respective pads of said scan-in I/O pads and scan-out I/O pads." Applicants point out at least seven of the eight scan-in and scan-out pins to registers 208A-208D of Shubat et al. are not to a scan-out in scan-in I/O pad.

In a fourth example, Shubat et al. does not teach: "preventing utilization of the entire failing macro-circuit." Applicants respectfully remind the Examiner, that he has equated Applicants "macro-circuits" with Shubat et al. memory instances, and no memory instance in Shubat et al. is entirely prevented from being used, just the failing redundant memory elements of the instance.

Based on the preceding arguments, Applicants respectfully maintain that Shubat does not anticipate claim 1, and that claim 1 is in condition for allowance. Since claims 2, 3, 5 and 9 depend from claim 1, Applicants contend that claims 2, 3, 5 and 9 are likewise in condition for allowance.

As to claim 10, the Examiner stated, Shubat teaches providing an integrated circuit (202,

Fig. 3A) having a multiplicity of macro-circuits (memory instances 204A – 204D, Fig. 3A) arranged in one or more groups, each macro circuit of the same group having the same function, and a fuse bank containing fuses (Fuses Box 206, Fig. 3A), isolating said-macro-circuits from other circuits of said integrated circuit, testing each macro-circuit prior to a fuse programming operation (By scanning appropriate location information into the redundancy scan flip-flops 304 before the fuse data is entered (i.e., prior to laser-blowing the fuses) and scanning that information out on a field-by-field basis, redundant wordlines or bitlines in individual memory instances may be pre-tested easily), programming said fuses in said fuse bank in order to store data indicating at least which macro-circuits failed said testing step and preventing utilization of each failing macro-circuit during operation (registers 208A through 208D, Fig. 3A) of said integrated circuit based on the data stored in said fuse bank. (Abstract, Col. 2, I. 46 to col. 3, I. 37, col. 7, l. 47 to col. 8, l. 20, col. 9, ll. 56-65 col. 10, l. 49 to col. 11, l. 2, claim 22).

Applicants respectfully contend that the arguments presented *supra* with respect to claim 1 are applicable to claim 10. Applicants respectfully maintain that Shubat et al. does not anticipate claim 10, and that claim 10 is in condition for allowance. Since claims 11, 12, 14, 19 and 20 depend from claim 10, Applicants contend that claims 11, 12, 14, 19 and 20 are likewise in condition for allowance.

35 U.S.C. § 103(a)

The Examiner rejected claims 15 and 16 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Shubat et al. (US-6,363,020), hereinafter Shubat.

The Examiner rejected claims 4, 7, 17 and 18 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Shubat et al. (US-6,363,020), hereinafter Shubat in view of Seitoh (US-6,829,181), hereinafter Seitoh.

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As to claims 4, 7, 8, 13, and 15-18, Applicants have argued *supra* in response to the Examiners § 102(b) rejection of claims 1 and 10 that claims 1 and 10 are allowable, since claims 4, 7 and 8 depends from claim 1 and claims 15-18 depend from claim 10, Applicants respectfully maintain that claims 4, 7, 8, 13, and 15-18 are in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0457 (IBM).

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